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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/908,941	07/20/2001	Masaki Hirase	010917	1043

23850 7590 07/07/2004

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/908,941	HIRASE ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *1 and 2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *3-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Currently claims 1-10 are pending in the application. Claims 1-2 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,303,458) in view of Krivokapic et al. (U.S. Patent No. 6,087,208).

Zhang et al. discloses the method of making a semiconductor device comprising:

forming an element partitioning trench (42) and a mask aligning trench (40) in a semiconductor substrate (10);

simultaneously depositing an insulation (referred to as both 40 and 50) in the element partitioning trench and the mask aligning trench, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

applying a protective mask (60) on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench (see Figure 5A)

etching the insulation deposited in the mask aligning trench to remove some of the insulation (see Figure 3B and column 4, lines 35-45); and

flattening an upper surface of the semiconductor substrate (see column 4, lines 55-60).

Zhang et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by chemical vapor deposition process consisting HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation of Zhang et al. layer by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim 4, Zhang et al. also discloses the method of forming a coating (30) on the semiconductor substrate, wherein the coating has a pattern of openings corresponding to the element partitioning trench and the mask aligning trench and etching the semiconductor substrate using the coating as a mask to form the element partitioning trench and the mask aligning trench, wherein the insulation depositing step includes depositing the insulation without removing the coating (see column 3, line 65 through column 4, line 20).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,303,458) and Krivokapic et al. (U.S. Patent No. 6,087,208) in view of Schoenfeld (U.S. Patent No. 6,127,245).

Zhang et al. and Krivokapic et al. disclose the method as claimed and rejected above including the steps of flattening by a chemical mechanical process, but do not disclose the method of flattening is performed rotary grinding. Schoenfeld discloses the method of utilizing a rotary grinder in CMP process (see column 5, lines 30-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a rotary grinding disc in the CMP process of the combined Zhang et al. and Krivokapic et al. in order to create a uniform flat surface that allows for ease of formation of subsequently formed devices.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,303,458), Krivokapic et al. (U.S. Patent No. 6,087,208), and Schoenfeld (U.S. Patent No. 6,127,245), in further view of Kuroi et al. (U.S. Patent No. 5,889,335).

The combined Zhang et al., Krivokapic et al., and Schoenfeld et al. disclose the method as claimed and rejected above including the method wherein the insulation is formed from oxide (40, 50), the coating is formed from silicon nitride (top portion of 30) and acts as and etching stopper (i.e. prevents etching of the underlying layer, see column 4, lines 10-15), the method further comprising the step of forming a oxide film (30) on the semiconductor substrate prior to the formation of the element partitioning

trench and the mask aligning trench, wherein the coating is formed on the oxide film (see column 3, line 65 through column 4, line 4).

The combined Zhang et al., Krivokapic et al., and Schoenfeld et al., do not expressly disclose the method of forming the substrate of silicon, or the method of forming the insulation of silicon oxide, or wherein the pad oxide layer that is formed prior to the forming of the silicon nitride layer coating is a silicon oxide.

Kuroi et al. discloses the method of utilizing silicon (1) as the substrate material, silicon oxide as the insulation material (2), and silicon oxide (3) as the pad oxide layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form these layers of these materials because they are preferred materials for their respective intended purposes. Silicon would be obvious to use as a substrate material because of the larger bandgap of the material which results in smaller leakage currents. Silicon oxide would be obvious to use as insulation material in isolation trenches because it is easy to form and chemically stable and has the expectation to insulate. Silicon oxide would be obvious to use as a pad oxide layer because it is easy to form and chemically stable and protects the underlying substrate during photolithographic processing.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. and Krivokapic et al. (U.S. Patent No. 6,087,208) in view of Kuroi et al. (U.S. Patent No. 5,889,335).

Zhang et al. discloses the method of manufacturing a semiconductor device, comprising;

forming an oxide film (30) on an upper surface of a semiconductor substrate;

forming a silicon nitride film (30) on the oxide film (see column 3, line 65 through column 4, line 4);

partially removing the silicon nitride film and the oxide film (see column 4, lines 10-19);

forming an element partitioning trench and a mask aligning trench by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein element partitioning trench and the mask aligning trench have substantially the same depths (see column 4, lines 4-35 and Figures1A, 1B);

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively (referred to as both 40 and 50);

coating the first insulation with a protective mask (60) to fully cover the element partitioning trench (see Figure 5a), wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

etching the second insulation so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation (see column 4, lines 45-55); and

removing the protective mask (see column 4, lines 55-60, and Figures 4A, 4B)

Zhang et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by chemical vapor deposition process consisting HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation of Zhang et al. layer by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

The combined Zhang et al. and Krivokapic et al. do not expressly disclose the method of forming the insulation of silicon oxide, or wherein the pad oxide layer that is formed prior to the forming of the silicon nitride layer coating is a silicon oxide.

Kuroi et al. discloses the method of utilizing silicon oxide as the insulation material (2), and silicon oxide (3) as the pad oxide layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form these layers of these materials because they are preferred materials for their respective intended purposes. Silicon oxide would be obvious to use as insulation material in isolation trenches because it is easy to form and chemically stable and has the expectation to insulate. Silicon oxide would be obvious to use as a pad oxide layer because it is easy to form and chemically stable and protects the underlying substrate during photolithographic processing.

In re claim 8, Zhang et al. further discloses the method wherein the first insulating and the second insulation are made of the same material (40, 50, see column 4, lines 30-35).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,303,458) in view of Krivokapic et al. (U.S. Patent No. 6,087,208).

In re claim 9, Zhang et al. discloses the method for manufacturing a semiconductor device, the method comprising:

Zhang et al. discloses the method of making a semiconductor device comprising:

forming an element partitioning trench (42) and a mask aligning trench (40) in a semiconductor substrate (10);

simultaneously depositing an insulation (referred to as both 40 and 50) in the element partitioning trench and the mask aligning trench;

applying a protective mask (60) on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench (see Figure 5A)

etching the insulation deposited in the mask aligning trench to remove some of the insulation (see Figure 3B and column 4, lines 35-45); and

flattening an upper surface of the semiconductor substrate (see column 4, lines 55-60).

Zhang et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma

chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by chemical vapor deposition process consisting HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation of Zhang et al. layer by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. and Krivokapic et al. (U.S. Patent No. 6,087,208) in view of Kuroi et al. (U.S. Patent No. 5,889,335).

Zhang et al. discloses the method of manufacturing a semiconductor device, comprising;

forming an oxide film (30) on an upper surface of a semiconductor substrate;

forming a silicon nitride film (30) on the oxide film (see column 3, line 65 through column 4, line 4);

partially removing the silicon nitride film and the oxide film (see column 4, lines 10-19);

forming an element partitioning trench and a mask aligning trench by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein element partitioning trench and the mask aligning trench have substantially the same depths (see column 4, lines 4-35 and Figures1A, 1B);

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively (referred to as both 40 and 50);

coating the first insulation with a protective mask (60) to fully cover the element partitioning trench (see Figure 5a);

etching the second insulation so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation (see column 4, lines 45-55); and

removing the protective mask (see column 4, lines 55-60, and Figures 4A, 4B)

Zhang et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by chemical vapor deposition process consisting HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation of Zhang et al. layer by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

The combined Zhang et al. and Krivokapic et al. do not expressly disclose the method of forming the insulation of silicon oxide, or wherein the pad oxide layer that is formed prior to the forming of the silicon nitride layer coating is a silicon oxide.

Kuroi et al. discloses the method of utilizing silicon oxide as the insulation material (2), and silicon oxide (3) as the pad oxide layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form these layers of these materials because they are preferred materials for their respective intended purposes. Silicon oxide would be obvious to use as insulation material in isolation trenches because it is easy to form and chemically stable and has the expectation to insulate. Silicon oxide would be obvious to use as a pad oxide layer because it is easy to form and chemically stable and protects the underlying substrate during photolithographic processing.

Response to Arguments

Applicant argues that the width of the mask 60 is less than that of the STI trench 42. The examiner notes that in Figure 5a it is clearly shown that the mask 60 fully covers the STI trench 42.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wolf et al. (Silicon Processing for the VLSI Era, Volume 1-Process Technology, 1986, Lattice Press, page 1) discloses the advantages to silicon substrates and silicon oxide.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmk

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800